

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S8	14	((hardware adj description adj language) HDL) and asynchronous and (((inter adj process) interprocess) adj communication) and clock and TCP and PLD and embedded and debugger	US_PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/15 13:32
S9	14	((hardware adj description adj language) HDL) and asynchronous and (((inter adj process) interprocess) adj communication) and clock and TCP and PLD and embedded and debugger and ((multiple plurality) same software same simulat\$6)	US_PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/15 13:35
S10	15	((hardware adj description adj language) HDL) and asynchronous and (((inter adj process) interprocess) adj communication) and clock and TCP and debug\$3 and ((multiple plurality) same software same simulat\$6)	US_PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/05/15 13:36
S11	17	cosimulation and asynchronous	US_PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/05 19:50

S12	575	simulation and (asynchronous same clock same (maximum threshold reference parameter))	US_PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/05 19:51
S13	35	simulation.ab. and (asynchronous same clock same (maximum threshold reference parameter))	US_PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/05 19:51
S14	6	simulation.ab. and (asynchronous same clock same (maximum threshold))	US_PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/05 19:53
S15	7	simulation.ab. and (asynchronous same delay same (maximum threshold))	US_PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/05 19:54
S16	0	(cosimulation coverification (co adj simulation)) and (asynchronous same delay same (maximum threshold))	US_PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/05 19:56
S17	0	(cosimulat\$5 coverificat\$5 (co adj simulat\$5)) and (asynchronous same delay same (maximum threshold))	US_PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/05 19:57
S18	1	((distributed parallel) adj simulat\$5) and (asynchronous same delay same (maximum threshold))	US_PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/05 19:57
S19	0	((distributed parallel) adj simulat\$5) and (asynchronous same clock same (maximum threshold))	US_PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/05 19:57

S20	8	(cosimulation coverification (co adj simulation)) and (asynchronous same clock same (maximum threshold))	US_PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/05 19:58
S23	0	cosimulation.ab. and (asynchronous same (limit threshold))	US_PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/06 12:28
S41	1	asynchronous same readahead	US_PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/19 17:34
S42	191	asynchronous same clock same cycle same limit	US_PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/19 17:35
S43	8	(asynchronous same clock same cycle same limit) and (circuit same simulation)	US_PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/19 17:36
S44	181	(asynchronous same clock same cycle same limit) and (circuit)	US_PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/19 17:38
S45	18	(asynchronous same clock same cycle same limit) and simulation	US_PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/19 17:38
S52	5	(asynchronous same circuit same simulation) and interprocess and HDL	US_PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/19 19:22

S53	5	(asynchronous same circuit same simulation) and interprocess and (VHDL HDL Verilog)	US_PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/19 19:22
S54	310	(asynchronous same circuit same simulation)	US_PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/19 19:23
S55	127	(asynchronous same circuit same simulation) and (HDL VHDL Verilog)	US_PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/19 19:23

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